

Fig. 1

Patent No. 4,923,260

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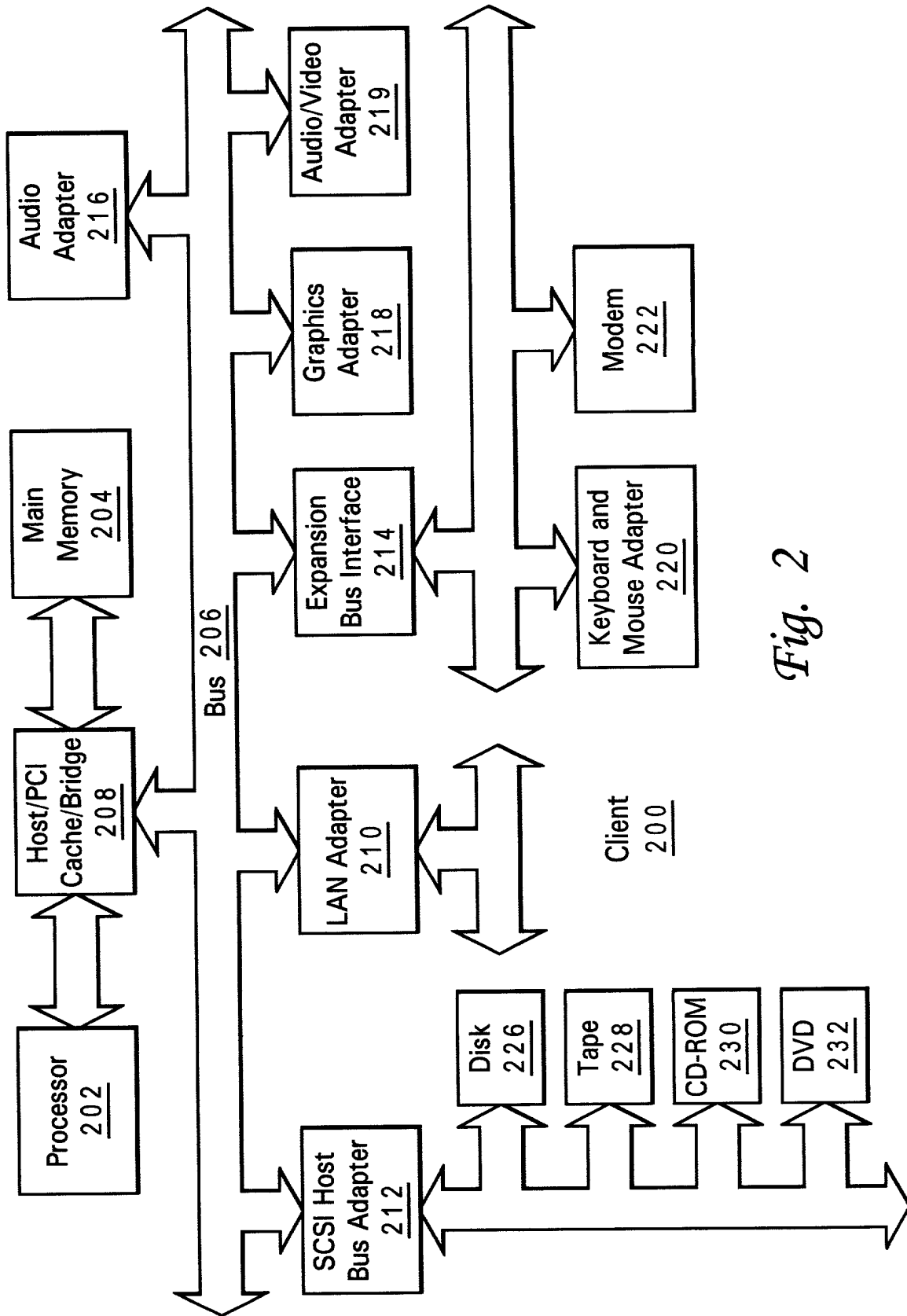


Fig. 2

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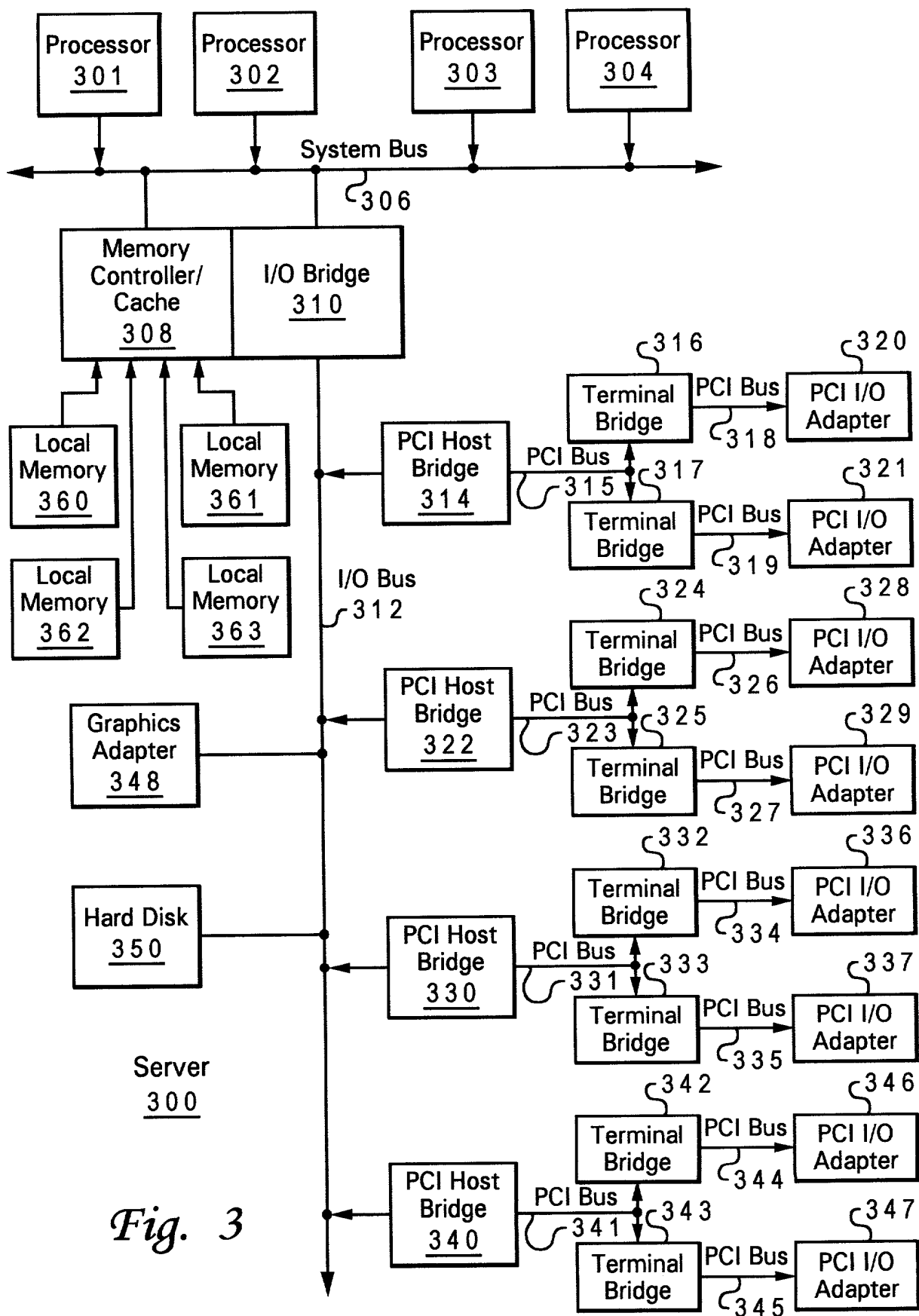
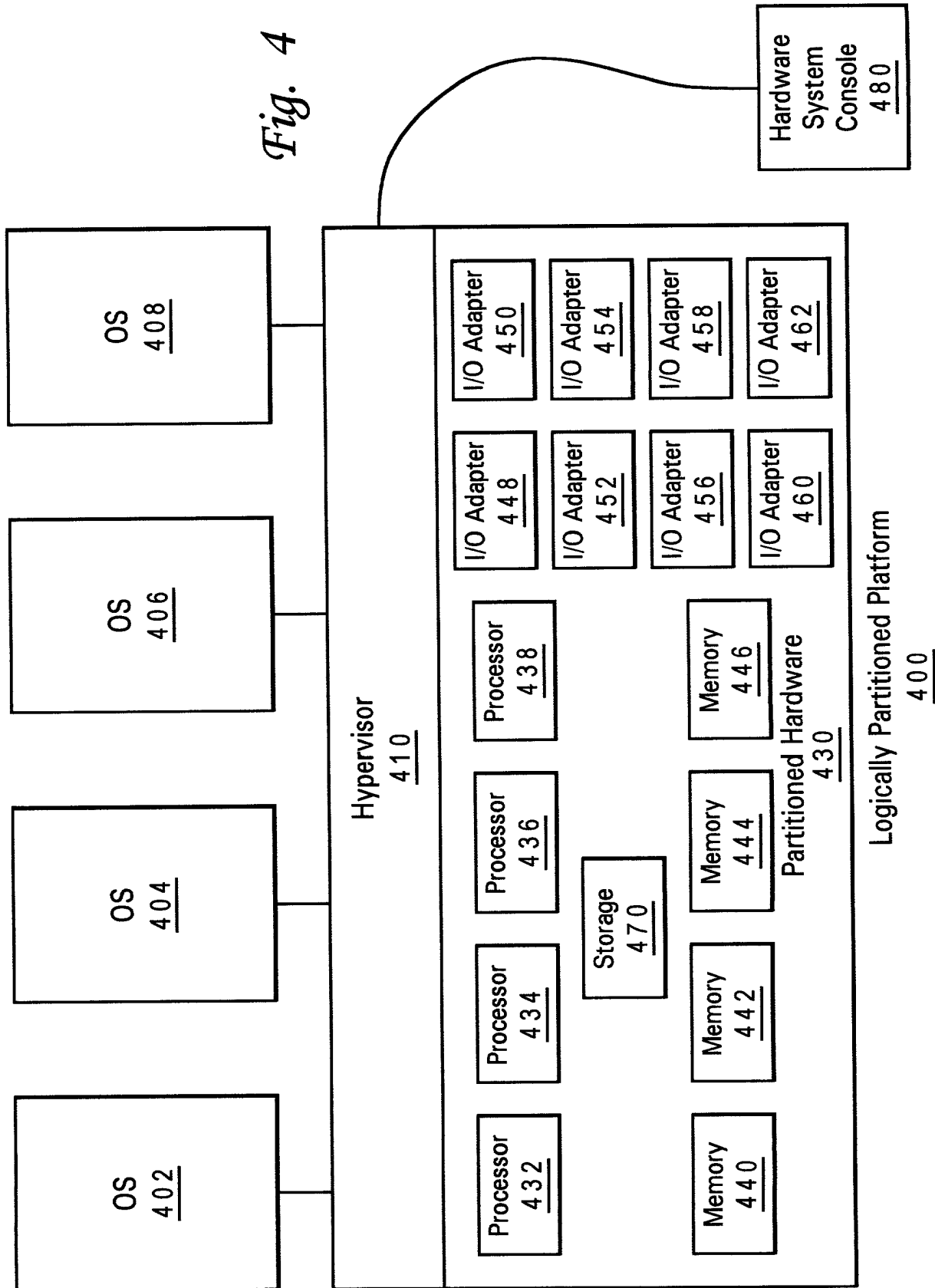


Fig. 3

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Fig. 4



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<u>IOA 1</u>	I/O bus DMA address 1-4
<u>IOA 2</u>	I/O bus DMA address 5-8
<u>IOA 3</u>	I/O bus DMA address 9-12

I/O Bus DMA Address Range Table

500

Fig. 5A

<u>OS 1</u>	IOA 1 IOA 3 Mem 1-20
<u>OS 2</u>	IOA 2 Mem 21-40

Fig. 5B

Allocation Table

520

Mem 5-8	I/O bus DMA addresses 1-4
Mem 11-13	I/O bus DMA addresses 9-11
Mem 25-26	I/O bus DMA addresses 5-6

TCE Table

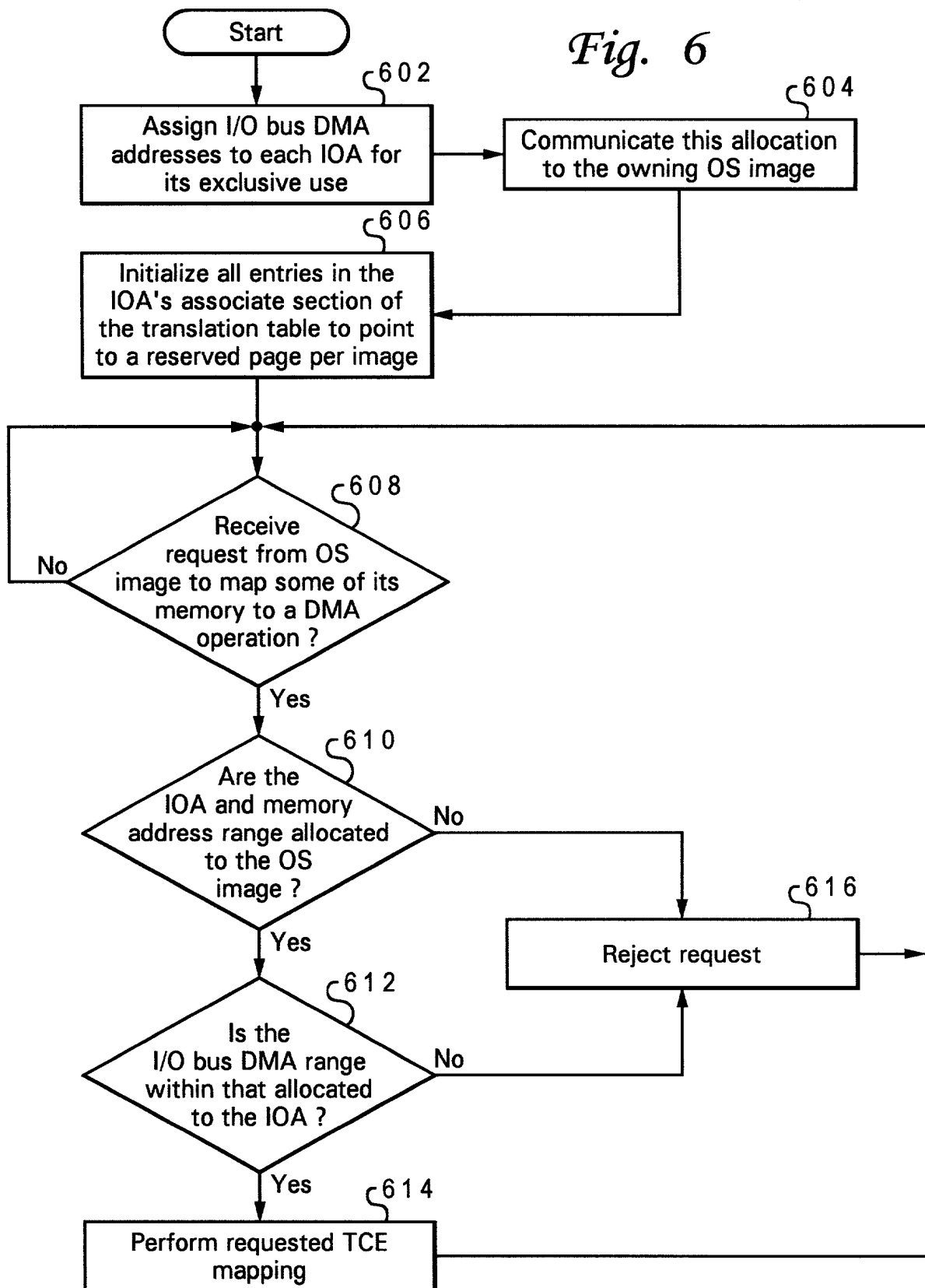
550

Fig. 5C

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Fig. 6



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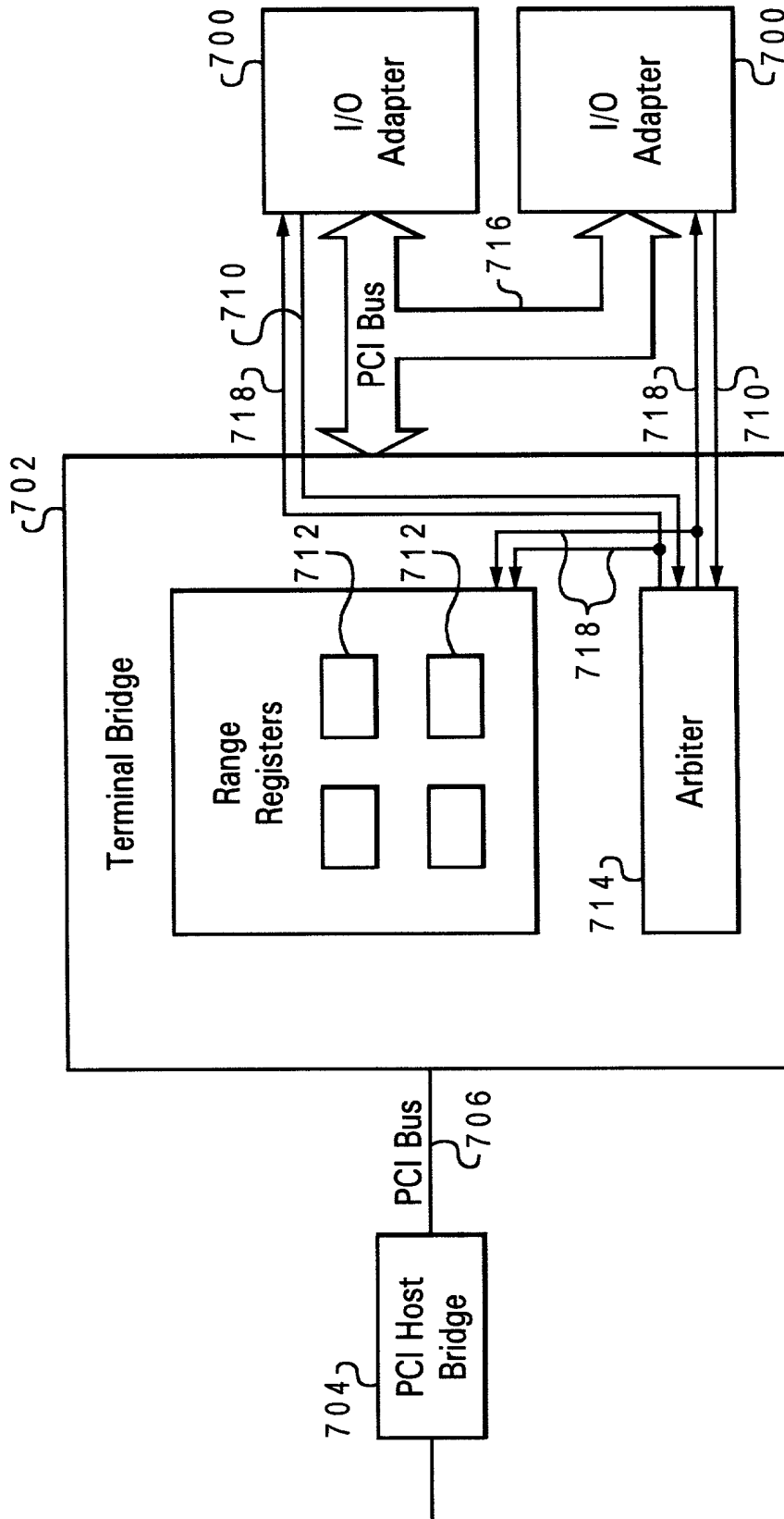


Fig. 7